Platinum Metals in Ohmic Contacts to III-V Semiconductors

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Platinum metals, particularly platinum and palladium, are used extensively in low resistance, relatively stable and laterally uniform ohmic contacts made to semiconductor devices formed from Group III and V elements. Palladium is primarily utilised as one component of a multilayer metallisation structure, improving adhesion to the semiconductor, while platinum is commonly used as a diffusion barrier to minimise interdiffusion between metal and semiconductor components. This paper describes the roles of platinum and palladium in ohmic contacts, gives examples of their typical utilisation and outlines the design considerations associated with the formation of reliable ohmic contacts.

Compound semiconductors formed from elements in Groups III and V (III-V) of the Periodic Table, such as GaAs and InP and related ternaries and quaternaries, have become important materials for a number of microelectronic and optoelectronic applications. These include field effect transistors (FET), junction field effect transistors (JFET), high electron mobility transistors (HEMT) and heterojunction bipolar transistors (HBT), as well as photonic devices, such as long-wavelength laser diodes, light-emitting diodes (LED) and photodetectors and solar cells. These devices are operated at high current densities and, as technology develops, are continually undergoing a reduction in size. In order to link the active regions of the semiconductor devices to the external circuit, contacts with low electrical resistance (ohmic contacts) are required. The small dimensions of these devices place severe processing constraints on the materials used in the construction of these ohmic contacts. The main requirements of ohmic contacts are that they should have low contact resistance, be thermally stable and have good adhesion and

Selected Ohmic Contacts to III-V Semiconductors

	Contact	Doping level, cm^{-3}	Minimum contact resistance, r_C, $\Omega\ cm^2$	Annealing temperature, °C	Refs.
n-Type	Pd-InP	1×10^{18}	7×10^{-5}	300 – 350	1, 2
	Pd/Ge/Au-InP	1×10^{17}	2.5×10^{-6}	300 – 375	3
	Pd/Ge-InP	1×10^{17}	6×10^{-6}	400 – 450	3
	Pd/Ge-GaAs	5×10^{18}	4×10^{-7}	400 – 415	4
p-Type	Pd/Pt/Au/Pd-InGaP/GaAs	3×10^{19}	$< 10^{-6}$	415 – 440	5
	Zn/Pd/Pt/Au-AlGaAs/GaAs		8.5×10^{-7}	440	6
	Ti/Pt/Au-InGaAs	5×10^{18}	6×10^{-7}	450	7
	Ti/Pt-InGaAs	5×10^{18}	4×10^{-6}	450	8
	Ti/Pt-InGaAs	1.5×10^{19}	3.4×10^{-8}	450	9
	Pd/Zn/Pd/Au-InP	2×10^{18}	7×10^{-5}	420 – 425	10

lateral uniformity. These are all directly affected by the microstructure of the contact.

Platinum metals are used extensively in ohmic contacts to III-V semiconductors, as diffusion barriers or reactive components in multilayer metallisation schemes. Examples of typical contacts are given in the Table, together with their minimum contact resistances.

Formation of Ohmic Contacts

Metal-semiconductor contacts can be divided into two types, based on their current-voltage characteristics. Contacts which show rectifying characteristics are called Schottky barriers or rectifying contacts, and contacts which have linear current-voltage behaviour are referred to as ohmic contacts. In practice, a contact is ohmic if the voltage drop across it is negligible compared with the voltage drop across the device or specimen – the contact is thus not affecting the current/voltage (I/V) characteristics of the device. There are several methods for forming low resistance ohmic contacts, but manufacture of the most common commercial contacts always involves the formation of a very heavily doped ($> 5 \times 10^{18}$ cm^{-3}) thin layer of semiconductor material on the semiconductor surface, immediately adjacent to the metal, see Figure 1. The depletion region produced at the interface between the metal and the semiconductor is then so thin that field emission or tunneling of charge carriers may take place, giving a contact with a very low resistance at zero bias.

Production of the highly doped surface can be achieved in two ways. One method involves growing a heavily doped epitaxial layer, for example, by chemical vapour deposition (CVD) on the semiconductor prior to metal deposition. The epitaxial layer is often a material with a lower bandgap, such as $In_{0.53}Ga_{0.47}As$ ($E_g = 0.75$ eV) which is lattice matched to InP, or a graded $In_xGa_{1-x}As$ layer (graded to InAs at the surface) (11). These contacts should not, at least in theory, require subsequent annealing and are therefore referred to as non-alloyed contacts. In practice, most of these contacts are still annealed to attain optimum values of contact resistance.

The other method of producing the doped, thin layered surfaces is by using an external dopant. The dopant, for example, zinc for *p*-type and germanium for *n*-type semiconductors, is deposited as a thin layer (of a few to tens of nanometres in thickness) on the semiconductor by electron beam evaporation and is usually driven into the semiconductor by solid state diffusion, which requires heating the contact. These contacts are termed alloyed contacts and the dopant metal is usually part of a multilayer metallisation scheme, the other possible metal layers including adhesion layers, diffusion barriers and capping layers to prevent oxidation during annealing.

In designing contacts to III-V semiconductors a number of factors have to be considered (12), the most important probably being the contact resistance. Several other important factors have

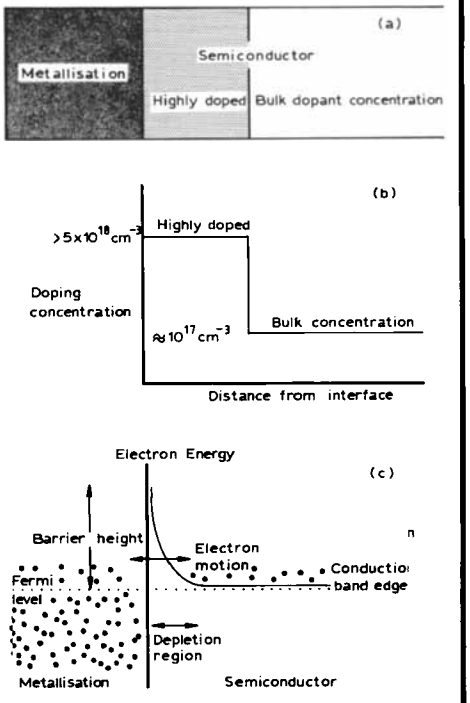

Fig. 1(a) Schematic of an ohmic contact structure to an *n*-type semiconductor; (b) Simplified plot of doping concentration of semiconductor in (a); (c) Simplified energy band diagram of metallisation/semiconductor interface region

to be taken into account, as contacts should be stable over a wide temperature range, have good lateral uniformity and shallow diffusion depths. These aspects have become particularly important as device dimensions are continually being decreased in size. However, it is difficult to meet all the requirements in a given contact metallisation. In order to achieve low contact resistance, interdiffusion between the metallisation components and the semiconductor is needed and this can compromise contact stability and uniformity.

The electrical properties of ohmic contacts are defined by a specific contact resistance, r_C, (13):

$$r_C = (\delta V/\delta J)_{V=0} \quad (\Omega\ cm^2) \qquad (1)$$

where V is the voltage and J is the current density. For a homogeneous contact of area A with a uniform current density, the contact resistance R_C is simply:

$$R_C = r_C/A$$

The measured resistance R will be approximately equal to R_C for most sample geometries when $r_C \geq 10^{-2}\ \Omega\ cm^2$. For lower values of r_C, the spreading resistance of the semiconductor and the series resistance of the connecting wires and semiconductor substrate must be taken into account. Specific contact resistances of $< 10^{-4}\ \Omega\ cm^2$ are required for ohmic behaviour, although values in the 10^{-6} to $10^{-7}\ \Omega\ cm^2$ range are most desirable.

Platinum Metals in Ohmic Contacts

Palladium and platinum are common components in ohmic contact metallisation schemes to III-V semiconductors. Many of the original III-V ohmic contacts were gold-based and although these contacts possess low resistance values, they are plagued by problems of stability and uniformity of interface structures. Platinum metals based contacts are generally less reactive and produce more uniform interfaces. Common features of the platinum metals include ease of deposition, good oxidation resistance, relatively low reaction temperatures with III-V compound semiconductors (which greatly enhances contact adhesion to the semiconductor) and compound formation with both the Group III and Group V elements (12). Reactions which occur during annealing are quite similar and are summarised below:

(a) Palladium and platinum react with compound III-Vs at low temperatures to form metal-rich ternary phases. Many of these are amorphous, particularly those with InP.

(b) Annealing of the ternary phases results in their decomposition into binary phases and/or elemental species.

Portions of isothermal sections (at 600°C) of the phase diagrams, determined from bulk specimens for Pd-In-P, Pt-In-P, Pd-Ga-As and Pt-Ga-As systems are shown in Figures 2 and 3. Note, the similarities between the systems, particularly the three-phase region bounded by InP or GaAs, and the binary phases with the Group III and Group V elements. Annealing of thin palladium or platinum layers on the III-V semiconductor should then result in the formation of the phases in the three phase region.

Palladium in Ohmic Contacts

Palladium can be utilised on its own to form ohmic contacts to III-V semiconductors (for example, Pd/*n*-type InP with a contact resistance of $7 \times 10^{-5}\ \Omega\ cm^2$ (1, 2)). However, palladium is generally one component in a multilayer metallisation, where its primary functions are to serve as an adhesion layer and to initiate reactions with the underlying semiconductor. The annealing behaviour of a layer of palladium (several tens of nanometres thick) on InP or GaAs plays an important role in how the contact functions.

In the **Pd/InP system**, see Figure 2(a), an amorphous ternary phase ($Pd_{\approx 3}InP$) forms during palladium deposition and grows on annealing (17, 18). At ≈225°C, crystalline islands of cubic Pd_2InP ($L1_2$-type structure) begin to nucleate and grow at the amorphous layer/InP interface. After annealing at 225 to 275°C, Pd_2InP grows into a continuous, epitaxial layer (40–50 nm thick). Two other ternary phases, Pd_5InP and Pd_2InP(II) (of composition and structure similar to Pd_2InP) then form and also grow epitaxially. At 300 to 350°C, all the

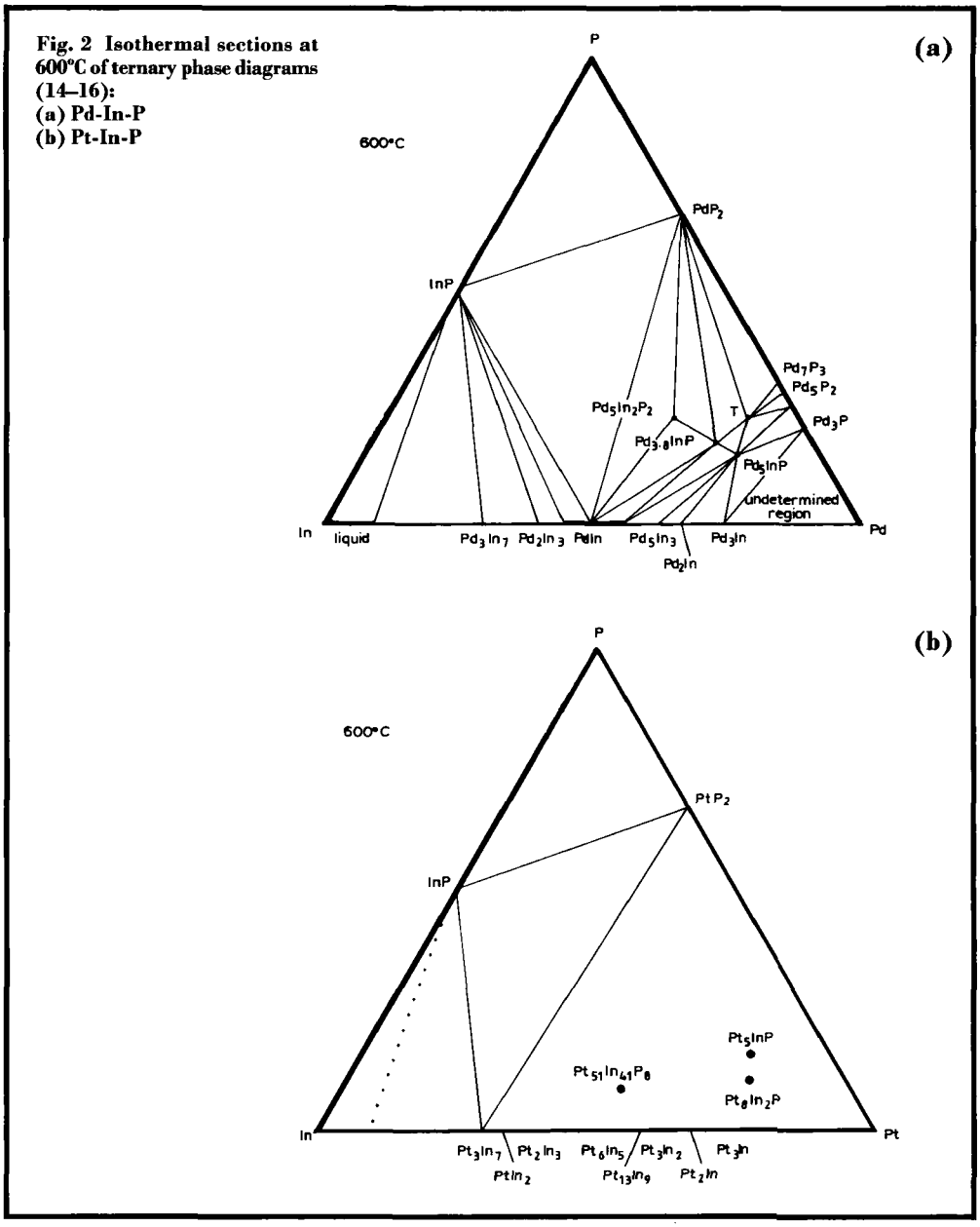

Fig. 2 Isothermal sections at 600°C of ternary phase diagrams (14–16):
(a) Pd-In-P
(b) Pt-In-P

palladium is consumed and Pd_2InP(II) is the only phase present on InP.

For the **Pd/GaAs system,** see Figure 3(a), a hexagonal ternary phase, $Pd_5(GaAs)_2$, forms and grows epitaxially on GaAs during palladium deposition (19, 20). Growth of this phase continues during subsequent annealing (< 250°C), with palladium being the dominant diffusing species. A second ternary phase, $Pd_4(GaAs)$, forms at higher annealing temperatures (up to ≈ 350°C) (19, 20). This phase also demonstrates an orientation relationship with GaAs. Growth of the ternary phases consumes the palladium by temperatures of ≈ 300 to 325°C.

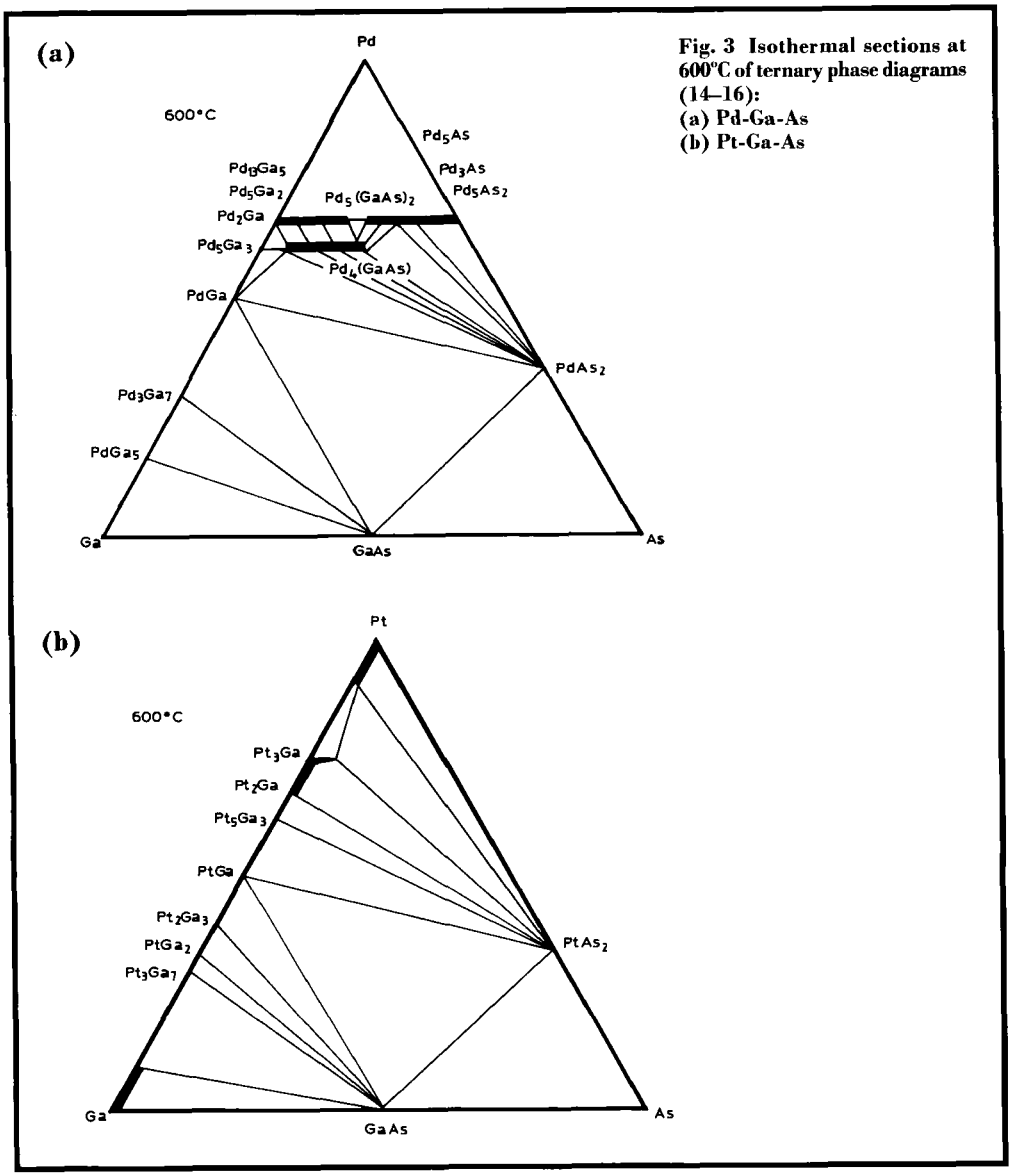

Fig. 3 Isothermal sections at 600°C of ternary phase diagrams (14–16):
(a) Pd-Ga-As
(b) Pt-Ga-As

Further annealing of palladium metallisations results in decomposition of the ternary phases and subsequent formation of binary compounds. In the case of GaAs: PdGa and $PdAs_2$ have been reported to form in one study (19), while Pd_2Ga and Pd_2As were reported in another study (20). According to the Pd-Ga-As phase diagram, Figure 3(a), PdGa and $PdAs_2$ are the stable phases in contact with GaAs.

Annealing samples of **Pd/InP** at temperatures $\geq 400°C$ results in decomposition of Pd_2InP(II) to PdIn and PdP_2 (17), which are the equilibrium phases in contact with InP (Fig. 2 (a)).

Specific Contacts

As mentioned above, palladium can be used by itself in ohmic contacts, however, its use in this way is rare. Instead, in practice, palladium is utilised as an integral component in many contacts, with its primary role being that of

an adhesion layer to the III-V semiconductor.

Ge/Pd One particular contact structure of interest is Ge/Pd, which was originally applied to *n*-type GaAs (21–24) (and later to InP, see below (3, 25)). Ohmic contact formation is based on a solid phase regrowth mechanism (21). According to this mechanism, films of two elements, M and M′ (palladium and germanium for this specific case) are deposited sequentially on a III-V semiconductor, AB (such as GaAs). At low annealing temperatures, the M metal film adjacent to the semiconductor reacts with AB to form a ternary phase M_xAB:

$$xM + AB \rightarrow M_xAB$$
$$4Pd + GaAs \rightarrow Pd_4GaAs$$

The second film (M′ or Ge) is chosen so that it drives the decomposition of M_xAB and forms a stable binary compound with M. M′ should also be a suitable dopant for AB.

$$(xy)M' + M_xAB \rightarrow AB + xMM'_y$$
$$4Ge + Pd_4GaAs \rightarrow GaAs + 4PdGe$$

AB regrows, doped with M′, epitaxially on the AB substrate. For the Ge/Pd-GaAs system annealing temperatures are in the range 300 to 500°C. In this contact, the onset of ohmic behaviour corresponds to the decomposition of Pd_4GaAs, which is driven by inward diffusion of germanium, and results in a highly doped regrown semiconductor layer. Specific contact resistances of the order of 5×10^{-7} to 1×10^{-6} Ω cm² have been achieved for both *n*-type and *p*-type GaAs, see the Table. Selecting the correct Ge:Pd ratio is crucial for fabricating uniform and stable contacts: the Ge:Pd atomic ratio must slightly exceed 1. This ensures that the only stable binary phase that forms is PdGe and this prevents the formation of other binary phases, such as Pd_2Ge, $PdAs_2$ and PdGa. In addition, any excess germanium is available for doping purposes.

For actual devices, comprising Pd/Ge contacts to *n*-type GaAs, a capping layer (for example, titanium/platinum) is needed to prevent the oxidation of germanium during subsequent device processing (4). Figure 4(a) shows an image of a platinum/titanium capped sample, while Figure 4(b) shows contact oxidation and deterioration for an uncapped sample. The Ti/Pt remains inert relative to the ohmic contact until annealing above ≈ 550°C, whereupon complex reactions result in rapid deterioration of the microstructure (26). Figure 4(c) shows the initial decomposition of PdGe at 550°C.

Pd/Ge-InP Similar Pd/Ge contacts have since been fabricated to *n*-type InP (3, 25). Pd_2InP

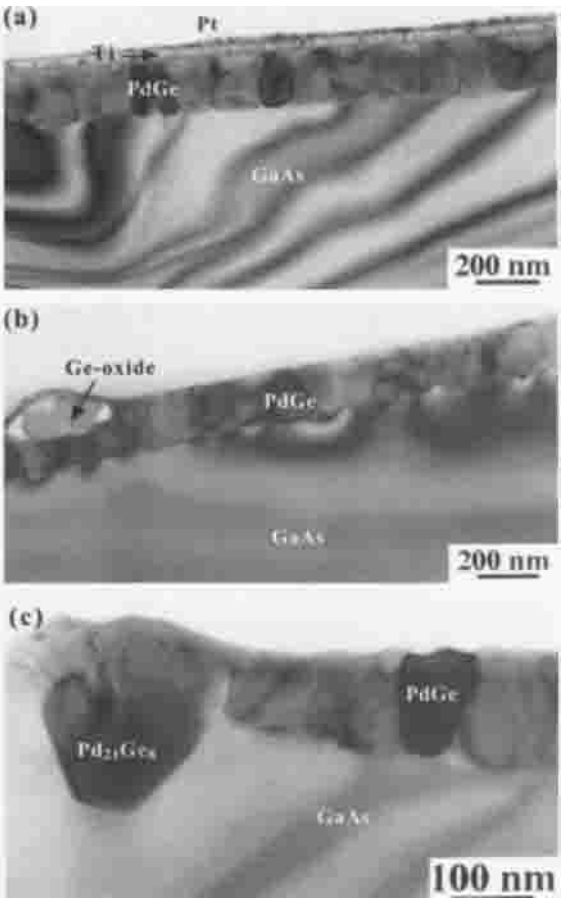

Fig. 4 TEM cross-section images of Pd/Ge contacts to *n*-type GaAs:
(a) with a Ti/Pt capping layer
(b) without a Ti/Pt capping layer (4)
(c) the contact in (a) has been annealed at 550°C and shows initial decomposition of PdGe (26)

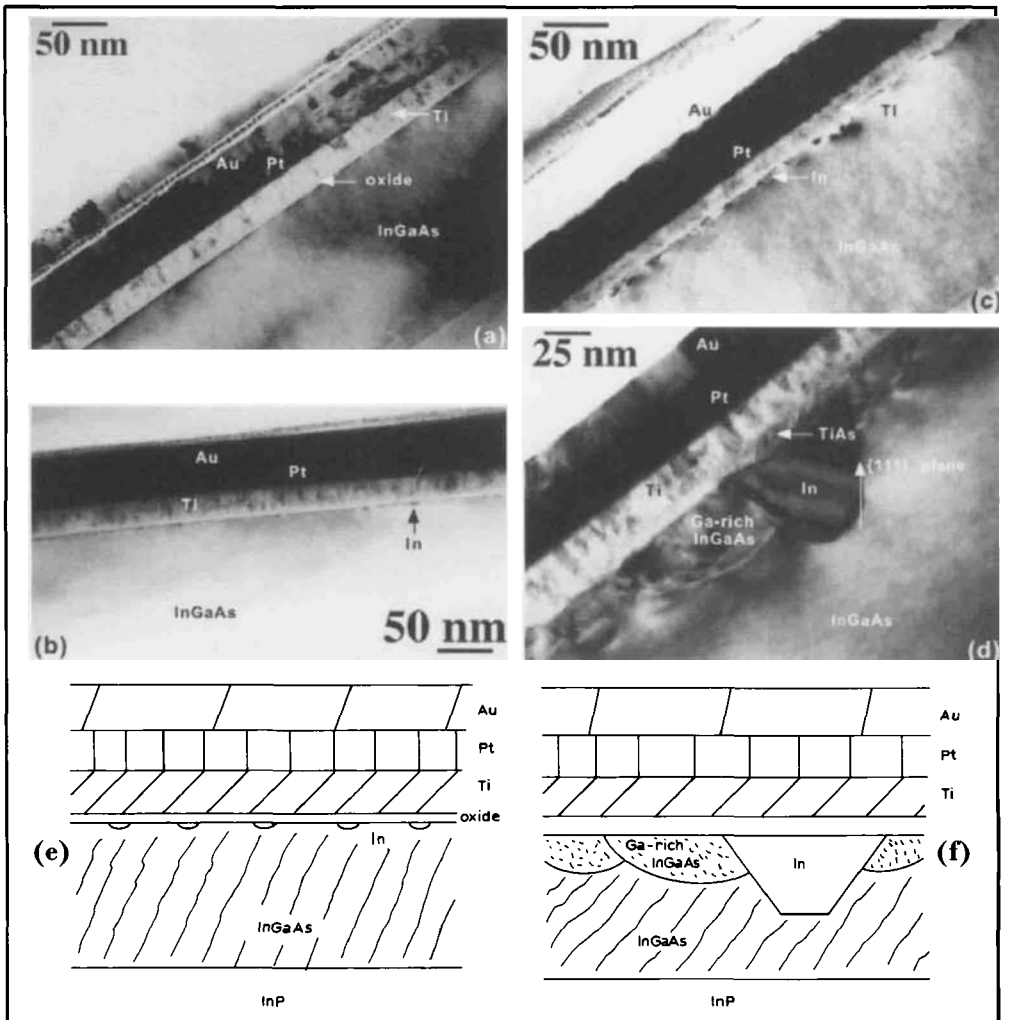

Fig. 5 TEM cross-section micrographs of Ti/Pt/Au contacts to *p*-type InGaAs (33): (a) as deposited; (b) 275°C; (c) 300°C; (d) 350°C; (e) and (f) are schematics of (b) and (d), respectively

forms initially followed by decomposition to PdGe and regrown InP. Contact resistances in the region of $10^{-6}\ \Omega\ cm^2$ have been achieved, see the Table.

Platinum in Ohmic Contacts

Reactions for the **Pt/InP system** are similar to those for the Pd/InP system. The main difference is that the reaction temperatures tend to be higher for platinum, which is not surprising as platinum has a higher melting point than palladium. Ternary amorphous phase formation begins at about 325°C, followed at ≈ 350°C by the formation of a crystalline ternary phase (Pt_5InP) (27). Pt_5InP does not form at the amorphous layer/semiconductor interface, but at the amorphous layer/metallisation interface, and as such exhibits no preferred orientation with the InP substrate. This is in contrast to Pd/InP where crystalline ternary phases nucleate, and then grow with a preferred orientation, at the semiconductor surface. A second ternary phase forms at 400°C which is followed by decomposition of both ternary phases to binary

phases at temperatures higher than 450°C. The final phases are $PtIn_2$ and PtP_2, which agree with those expected from the bulk Pt-In-P phase diagram, see Figure 2 (b) (14, 28).

Pt/GaAs reactions, see Figure 3(b), are similar to those of Pt/InP, with $PtAs_2$ and PtGa binary phases forming at temperatures ≈ 550°C (29–31).

Non-Alloyed Contacts The main application of platinum in ohmic contacts to III-V semiconductors (including InGaAs and InGaAsP) is in the so-called non-alloyed contacts. These usually consist of titanium and platinum layers, with or without a gold capping layer, deposited sequentially on the semiconductor (7, 8, 32). Gold, which can be deposited either before or after contact annealing, is needed to permit wire bonding and solder bonding of the device to a suitable submount. Deposition of gold prior to annealing permits deposition of all the metal layers in one sequence, without breaking the vacuum, although gold may reduce contact stability during subsequent annealing.

The titanium layer improves adhesion to the underlying semiconductor, while the platinum layer acts as a diffusion barrier for gold. Good contacts to a number of semiconductors have been obtained using this scheme, see the Table, giving contact resistance values depending very much on the initial doping levels in the semiconductors. The original doping levels in the semiconductors are generally quite high, so that many of these contacts are ohmic without being annealed or require very little annealing to attain ohmic behaviour, hence, the term non-alloyed contacts.

In reality, many of these contacts are annealed to optimise the electrical properties and therefore undergo fairly significant interfacial reactions, making the terminology "non-alloyed" something of a misnomer. An example of one of these contacts to *p*-type InP, and the interfacial reactions involved, is discussed below.

Ti/Pt/Au is the standard *p*-side metallisation used for a number of InP-based laser and optical wave-guide devices. *p*-Type InGaAs is grown as a lattice matched capping layer ($In_{0.53}Ga_{0.47}As$) on InP. Its low band gap (E_g ≈ 0.75 eV) relative to InP (E_g = 1.35 eV) and high dopant solubility (≈ 10^{19} cm^{-3} for zinc) permit the formation of low resistance contacts. Specific contact resistances as low as 3×10^{-8} Ω cm^2 (for high doping levels) have been reported, see the Table.

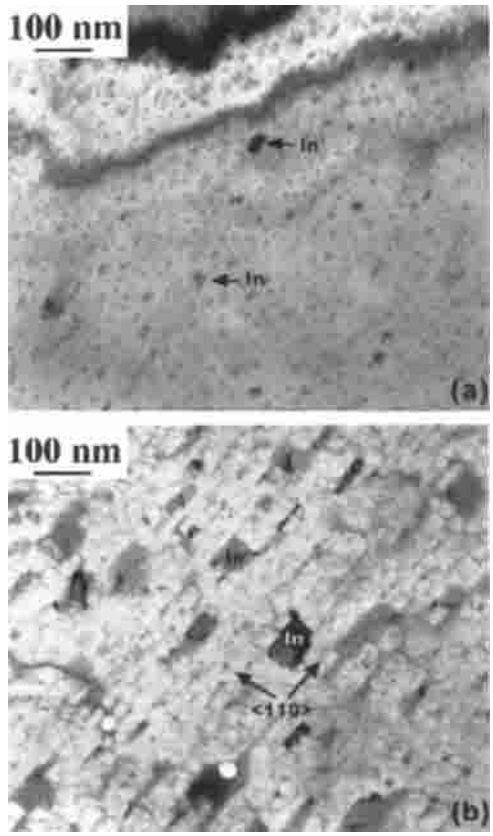

Fig. 6 TEM plan view images of indium particles at the Ti/InGaAs interface (33): (a) 275°C and (b) 350°C

A series of TEM cross-section micrographs, showing microstructure development during annealing are shown in Figure 5 (33). Reaction between titanium and InGaAs begins at ≈ 275°C and shows up as small dark contrast features at the Ti/InGaAs interface, Figure 5(b). These have been identified as metallic indium particles, which nucleate uniformly across the Ti/InGaAs interface and grow to ≈ 100 nm in size, see Figures 5(c) and 5(d). The indium particles are pyramidal in shape and grow along low energy {110} and {111} planes, Figures

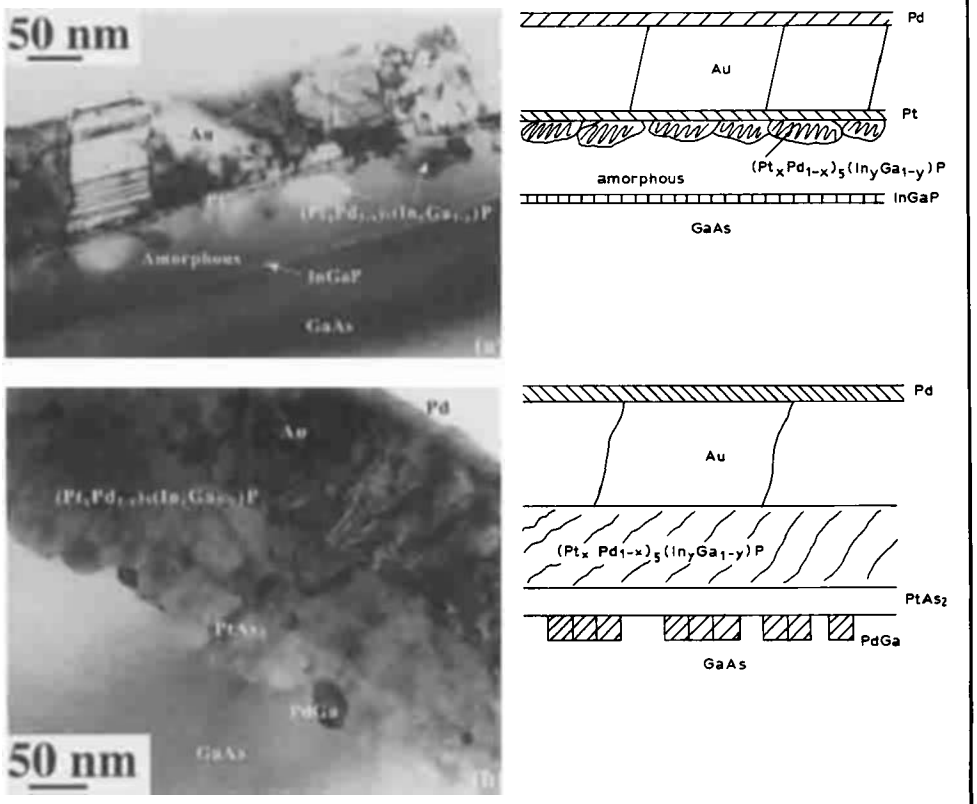

Fig. 7 TEM cross-section images and related schematics of Pd/Pt/Au/Pd contact to an InGaP/GaAs heterojunction bipolar transistor (5): (a) as deposited and (b) annealed at 440°C

5(d) and 6. Indium is a low melting point metal (157°C), which can dissolve up to ≈ 1.4 weight per cent gallium and up to ≈ 1 weight per cent zinc (the dopant in InGaAs). Both the gallium and zinc impurities lower the melting point of indium, which can affect the long term stability of devices. TiAs also forms at the Ti/InGaAs interface and thickens with increasing annealing temperature, see Figure 5(d). Depletion of indium and arsenic from the InGaAs layers results in the formation of gallium-rich InGaAs.

Platinum is an effective barrier, preventing inward diffusion of gold and outward diffusion of the Group III elements (indium and gallium), up to annealing temperatures of 450°C. At higher temperature significant interdiffusion between titanium and platinum occurs.

Some metallisations incorporate both palladium and platinum. One example was given previously (Pd/Ge/Ti/Pt to *n*-type GaAs, in Figure 4(a)), although the platinum was essentially inert and acted solely as a capping layer. However, in some instances, both palladium and platinum participate in metallisation/semiconductor reactions. This is shown in both Figures 7(a) and 7(b) for a multilayer *p*-contact **Pd/Pt/Au/Pd**, utilised for InGaP/GaAs heterojunction bipolar transistors (HBT) (5). The metal layers are deposited directly onto the emitter layer (InGaP) of the HBT, with palladium and platinum reacting with and consuming the InGaP during annealing to form an ohmic contact with the underlying base material (*p*-type GaAs). Lateral uniformity is particularly

important because of the thin nature of the base layer (< 100 nm). An outer layer of palladium protects the gold during subsequent device processing; dry etching sputters the gold but not the palladium. The doping level in the base layer is high enough (> 10^{19} cm^{-3}) that additional dopant is not required to achieve low contact resistances. The initial reaction between palladium and platinum and InGaP results in the formation of a 5-component amorphous layer (Pd, Pt, In, Ga and P), which crystallises to $(Pt_xPd_{1-x})_5(In_yGa_{1-y})P$ $(0 \leq x, y \leq 1)$ at the Pt/amorphous layer interface. Annealing at temperatures ≥ 415°C results in the complete consumption of InGaP and partial decomposition of the GaAs base layer, resulting in a relatively uniform contact consisting of $(Pt_xPd_{1-x})_5(In_yGa_{1-y})P$, $PtAs_2$ and PdGa, see Figure 7 (b). In this structure, contact resistance values < 10^{-6} Ω cm^2 are attainable.

Summary

Platinum and palladium are common components in ohmic contacts to III-V semiconductors. The metals react readily with the semiconductor at relatively low temperatures, forming ternary phases initially, followed by binary phase formation. Palladium is utilised primarily as an adhesion layer to the semiconductor, while the major role of platinum is as a diffusion barrier. In both cases, palladium and platinum act to improve contact stability and hence the reliability of the device to which they are attached.

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Platinum Dye Used in Electroluminescent Devices

Electroluminescent devices (LEDs) convert electricity to light and are increasingly used in, for example, flat-panel displays. They are usually made by sandwiching a layer of semiconductor between one electrode with a high work function (a source of holes) and an electrode with a low work function (an electron source). In the presence of an applied electric field an electron-hole exciton is formed (both singlet and triplet states) and the radiative recombination of the (singlet) exciton generates a photon that re-appears as visible light emitted from the device.

The current trend is towards the development of polymeric electroluminescent material because of the processing advantages. There is also a need to improve the overall energy conversion efficiency of LEDs, which is typically of the order of 1 per cent. One approach to the latter problem has been to introduce luminescent dyes into the host semiconductor material. Provided that the absorption spectrum of the dye overlaps well with the emission spectrum of the host material, efficient energy-transfer from the host to the dye can occur. However, only the singlet exciton states (approximately 25 per cent of the total) can be used in the additional fluorescent emission.

Now, workers from Princeton University and the University of Southern California have demonstrated improved light emission efficiencies by using a phosphorescent dye in the semiconductor host (M. A. Baldo, D. F. O'Brien, Y. You, A. Shoustikov, S. Sibley, M. E. Thompson and S. R. Forrest, "Highly Efficient Phosphorescent Emission from Organic Electroluminescent Devices", *Nature*, 1998, **395**, (6698), 151–154). The phosphorescent dye, 2,3,7,8,12,13,17,18-octaethyl-21H,23H-porphine platinum(II) (PtOEP), enables both singlet and triplet exciton states to be used in the light-emission process, and external energy conversion efficiencies of up to 4 per cent have been achieved.

PtOEP is relatively well-known as a red-emitting phosphorescent dye and in comparison with other compounds with saturated red-emission, PtOEP possesses quantum and power efficiencies that are superior by at least an order of magnitude. The presence of the heavy platinum atom in the porphine ring increases the spin-orbit coupling of the molecule, the triplet state gains additional singlet character and vice versa. This also enhances the efficiency of intersystem crossing from the first singlet excited state to the triplet excited state. Thus the enhanced phosphorescent light emission from the PtOEP adds significantly to the overall light-emitting process in the LED. The work also establishes the utility of PtOEP as a probe of triplet behaviour and energy-transfer in organic solid-state systems.

R. J. POTTER

International Symposium on Iridium

There will be an International Symposium on Iridium held at the Annual Meeting of The Minerals, Metals and Materials Society (TMS) in Nashville, Tennessee, U.S.A., from March 11th to 17th, 2000.

The symposium will address all aspects of the metallurgy, production, and applications for iridium and iridium-containing materials. Particular attention will be given to refining and recycling; processing iridium compounds; the processing, structure, and properties of iridium and its alloys; iridium coating technology; component design and applications and iridium as an alloying element in metallic and intermetallic systems. It is anticipated that the proceedings of the symposium will be published.

Evan Ohriner of Oak Ridge National Laboratory is the Primary Organiser of the Symposium; H. Harada, National Research Institute for Metals, Japan; R. D. Lanam, Engelhard-CLAL, U.S.A. and P. Panfilov, Ural State University, Ekaterinburg, Russia are the co-organisers.

Abstracts of papers should be submitted by June 15th 1999 to http://www.tms.org/cms., or contact the Primary Organiser: E. K. Ohriner, Oak Ridge National Laboratory, P.O. Box 2008, MS 6083, Bldg. 4508, Oak Ridge, TN 37831-6083, U.S.A.; telephone: +1-(423)-574-8519; fax: +1-(423) 574-4357; e-mail: ohrinerek@ornl.gov.